

[54] **CASCADABLE DIGITAL FILTER  
PROCESSOR EMPLOYING MOVING  
COEFFICIENTS**

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[57] **ABSTRACT**

A digital filter processor employs four multiplier-accumulator cells and an output accumulator for receiving and accumulating all cell outputs. Data is provided to all cells in parallel, and finite impulse coefficients are applied serially to all cells. A plurality of registers and at least one multiplexer interconnect the cells for transmitting the coefficients between cells. The registers can be employed for sample rate reduction or decimation. A plurality of processors can be cascaded for processing an increased number of coefficients without a reduction in sample time. Alternatively, data can be recycled in a processor to accommodate a number of coefficients greater than the number of cells at a reduced sampled sample rate. A cell address is provided for selecting cell outputs during the reading of the filtered/processed data.

11 Claims, 12 Drawing Sheets

